or a conventional metal gate material such as tungsten (W). The deposit of the gate electrode layer **32** is excessive and must be partially removed by a subtractive process such as CMP stopping on the top of the exterior masking layer **126** (e.g. SiGe layer **126**). Alternatively, the gate electrode layer **32** can be etched back.

[**0114**] Step 14: Form Recess of Sacrificial Exterior Spacer Layer Near Gate

[**0115**] **FIG. 3M** shows the device **60** of **FIG. 3L** after recesses **130** have been formed by selective RIE etching on either side of the gate electrode **32** and the inner sidewall spacers **30** and internal etch stop film **28** down to the first etch stop layer **20**. The recess **120** has been formed by anisotropically etching back the sacrificial outside spacer layer **124** between the internal etch stop film **28** and the exterior masking layer **126**. The recess **130** has been formed by etching back the sacrificial outside spacer layer **124** using the exterior masking layer **126** as the mask with an etchant which is selective to remove the material of the sacrificial outside spacer layer **124** (which may be silicon nitride or the like) while not attacking the exterior masking layer **126** (which may be SiGe or the like.) The etching process can be an anisotropic RIE process selective to removal of exposed silicon nitride of the sacrificial outside spacer layer **124**, while not attacking the material (e.g. silicon oxide) of the internal etch stop film **28** and the exterior masking layer **126**.

[**0116**] Step 15: Strip Away Exterior Masking Layer.

[**0117**] **FIG. 3N** shows the device **50** of **FIG. 3M** after stripping away the exterior masking layer **126**, thereby exposing the sacrificial outside spacer layer **124**. The method of removing the SiGe layer **126** is a non-hydrogen containing etch gas mixture. The etch may be a plasma etch and continues through the SiGe selective to Si. In this case the poly-Si gate will not be etched. (Here if one were to use silicon oxide as the sacrificial outside spacer layer **124**, instead of SiGe in step 6 of the fifth embodiment, the etching of the silicon oxide of the sacrificial outside spacer layer **124** the top of silicon nitride exterior masking layer **126**, may attack the internal etch stop film **28** (silicon oxide (SiO_2)) on the silicon nitride inner spacer sidewall **30**.

[**0118**] Step 16: Remove Exposed Portions of Etch Stop Layer

[**0119**] **FIG. 3O** shows the device **60** of **FIG. 3N** after a selective, anisotropic, RIE step using sacrificial outside spacer layer **124** as a mask to remove the exposed portion of the etch stop layer **20** (preferably composed of SiO_2) stopping on the then exposed surface of raised Si layer **18**.

[**0120**] Step 17: Extend Recess and Lower Height of Gate Electrode

[**0121**] **FIG. 3O** also shows the device **60** after, a different selective, anisotropic, RIE step is performed, also using the sacrificial outside spacer layer **124** as a mask, to remove the exposed portion of the raised silicon layer **18** stopping on the thin SiGe layer **16** and leaving a recess **140** below where recess **130** had been in **FIG. 3N**. At the same time, the height of the gate **32** is lowered to an equal degree to the raised silicon layer **18** forming a shortened gate **32"**, leaving the inner spacers **30** and the internal etch stop film **28** extending thereabove. In addition, the regions RE of the SiGe layer **16** are exposed between the raised silicon structures **18** and the gate **32"**.

[**0122**] Step 18: Strip Sacrificial Exterior Spacer Layer

[**0123**] **FIG. 3O** also shows the device **60** after an RIE step is performed to etch the exposed portion of the strip the sacrificial outside spacer layer **124** (preferably composed of silicon nitride) leaving the surface of the etch stop layer **20** exposed.

[**0124**] Step 19: Strip First Etch Stop Layer

[**0125**] **FIG. 3P** shows the device **50** of **FIG. 3O** with the gate electrode **155** shown, in an intermediate stage of completion, after stripping the remainder of the first etch stop layer **20** (which had been protected by the sacrificial outside spacer layer **124**) by an anisotropic RIE etching step. This leaves the surface of the raised silicon layer **18** exposed. If the first etch stop layer **20** is composed of silicon oxide (SiO_2), an anisotropic RIE step is performed to strip the etch stop layer **20**. This etching step may also etch away some of the exposed portions of the internal etch stop film **28**, which is exposed by the formation of the recess **129** in **FIG. 3M**, recess **130** in **FIG. 3N** and recess **140** in **FIG. 3O**.

[**0126**] Step 20: Lower Inner Sidewall Spacers

[**0127**] **FIG. 3Q** also shows the device **60** of **FIG. 3P** after performing an etch to lower the inner sidewall spacers **30** to the level of the gate electrode **32"**, which was lowered in step 17.

[**0128**] The etch is preferably a wet etch if the inner sidewall spacers **30** are composed of silicon nitride.

[**0129**] In the above etching steps, the internal etch stop film **28** prevents etching into the inner sidewall spacer **30**.

[**0130**] Step 21: Strip Internal Etch Stop Film

[**0131**] **FIG. 3R** shows the device **60** of **FIG. 3Q** after removal of the remainder of the internal etch stop film **28** leaving the sidewall spacers exposed adjacent to the gate electrode **165**. If the internal etch stop film **28** is composed of silicon oxide (SiO_2) the preferred method of stripping thereof is to perform a wet etch with a hydrogen fluoride bath.

[**0132**] Step 22: Halo Ion-Implantation

[**0133**] **FIG. 3S** shows the device **60** of **FIG. 3R** after angled halo ion-implantation under the edges of the gate electrode **32**

[**0134**] Step 23: Extension Ion-Implantation

[**0135**] **FIG. 3T** shows the device **60** of **FIG. 3S** after extension ion-implantation with a vertical angle into the exposed surfaces of the device **60**.

[**0136**] Step 24: Form External Sidewall Spacer **FIG. 3U** shows the device **60** of **FIG. 3T** after formation of external sidewall spacers **36** on the outer sidewalls of inner sidewall spacers **30**. The external sidewall spacers **36** are preferably composed of silicon nitride to control S/D diffusion.

[**0137**] Step 25: S/D Implantation

[**0138**] **FIG. 3V** shows the device **60** of **FIG. 3U** after a S/D ion implant of source/drain dopant into the raised Source/Drain (RSD) regions **18** on either side of the external sidewall spacers **36**, as will be well understood by those skilled in the art.